Refine Search

Search Results -

Terms	Documents
L2 or L4	54

Database:

US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L5

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Monday, September 27, 2004 Printable Copy Create Case

Set Name side by side	**Query**	**Hit Count**	**Set Name** result set
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR		
L5	l2 or L4	54	L5
L4	L3 same (compar$3 near10 monitor$3)	36	L4
L3	generat$3 same trigger same output same condition	11207	L3
L2	compar$3 same (trigger adj1 condition) same bus	20	L2
L1	compar$3 near5 (trigger adj1 condition) near10 bus	2	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L5	0

Database:
- US Pre-Grant Publication Full-Text Database
- US Patents Full-Text Database
- US OCR Full-Text Database
- EPO Abstracts Database
- JPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Search: L6

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Monday, September 27, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
L6	L5	0	L6
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR		
L5	l2 or L4	54	L5
L4	L3 same (compar$3 near10 monitor$3)	36	L4
L3	generat$3 same trigger same output same condition	11207	L3
L2	compar$3 same (trigger adj1 condition) same bus	20	L2
L1	compar$3 near5 (trigger adj1 condition) near10 bus	2	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
(345/10 |345/700 |717/128 |717/129 |710/100 |710/52 |712/33 |712/35 |713/502 |714/47 |714/30 |714/25 |714/45 |714/726 |714/39).ccls.	7950

Database:

US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L7

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Monday, September 27, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Se Nar resı se
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR		
L7	714/47,30,25,45,726,39;710/100,52;712/33,35;717/128,129;713/502;345/10,700.ccls.	7950	L
	DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
L6	L5	0	L
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR		
L5	l2 or L4	54	L
L4	L3 same (compar$3 near10 monitor$3)	36	L
L3	generat$3 same trigger same output same condition	11207	L
L2	compar$3 same (trigger adj1 condition) same bus	20	L
L1	compar$3 near5 (trigger adj1 condition) near10 bus	2	L

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L5 and L7	9

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L8

Refine Search

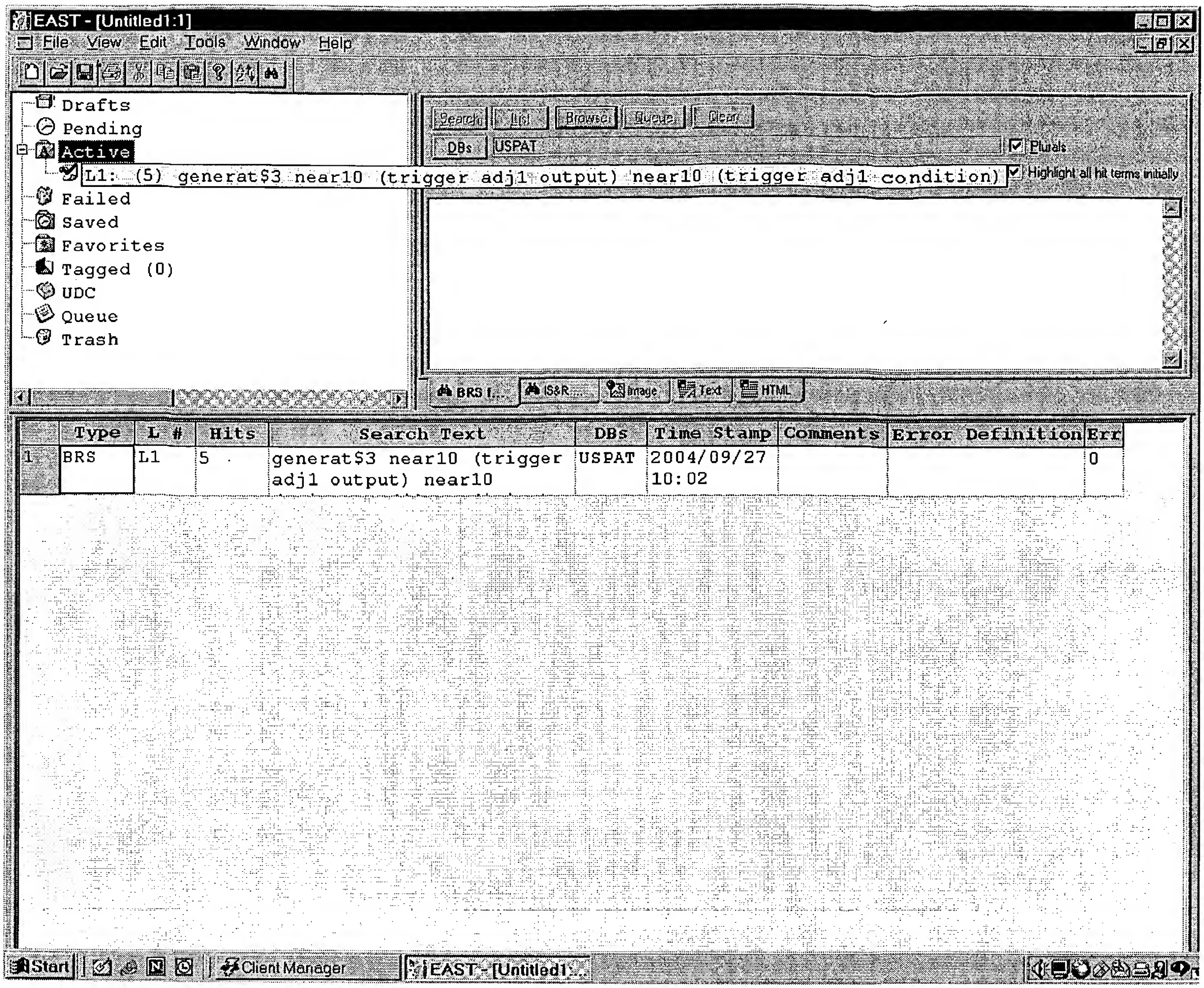
Recall Text Clear Interrupt

Search History

DATE: Monday, September 27, 2004 Printable Copy Create Case

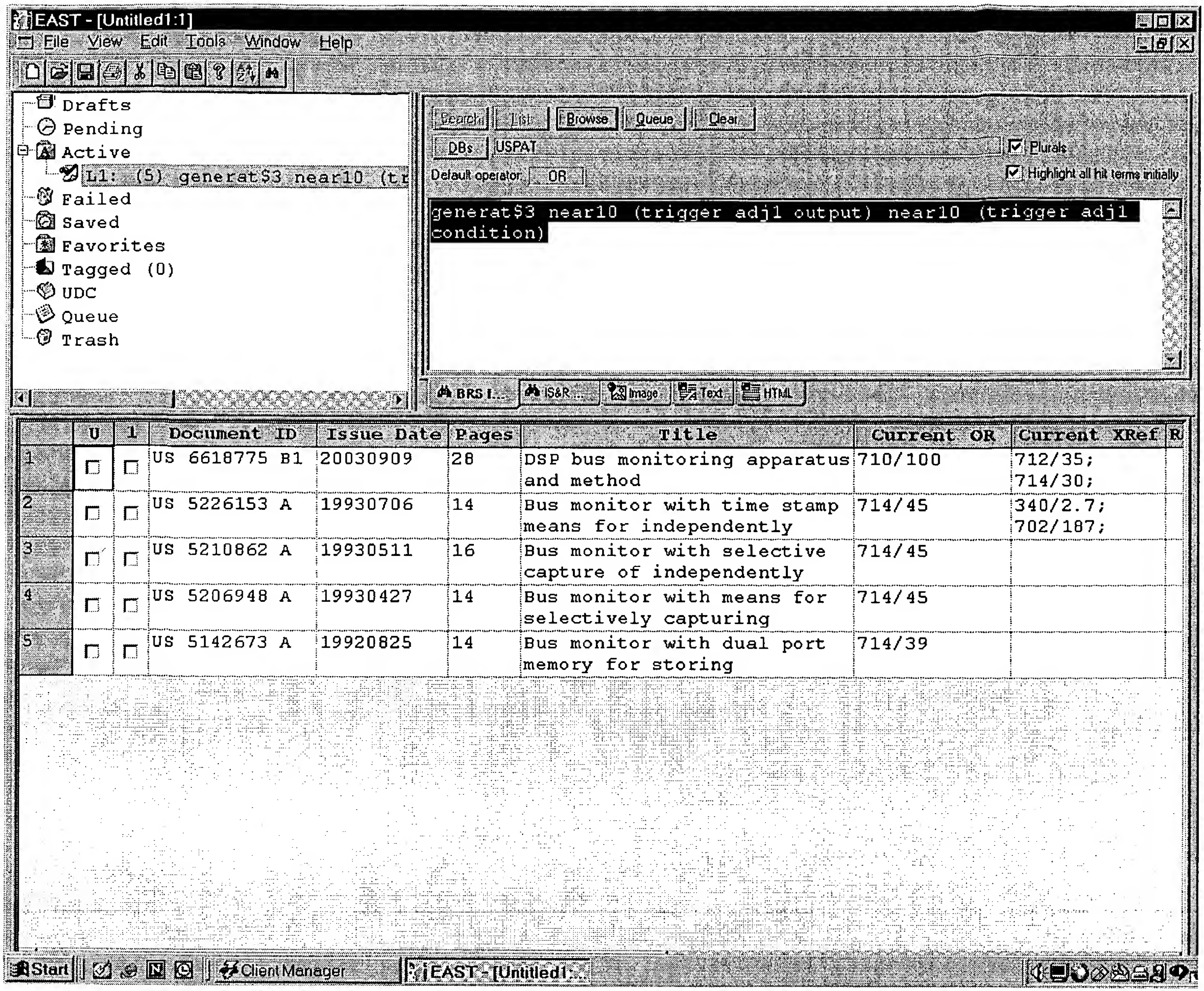
Set Name side by side	**Query**	**Hit Count**	**Se Nar** res se
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR		
L8	l5 and L7	9	L
L7	714/47,30,25,45,726,39;710/100,52;712/33,35;717/128,129;713/502;345/10,700.ccls.	7950	L
	DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
L6	L5	0	L
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR		
L5	l2 or L4	54	L
L4	L3 same (compar$3 near10 monitor$3)	36	L
L3	generat$3 same trigger same output same condition	11207	L
L2	compar$3 same (trigger adj1 condition) same bus	20	L
L1	compar$3 near5 (trigger adj1 condition) near10 bus	2	L

END OF SEARCH HISTORY



L1: (5) generat$3 near10 (trigger adj1 output) near10 (trigger adj1 condition)

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Err
1	BRS	L1	5	generat$3 near10 (trigger adj1 output) near10	USPAT	2004/09/27 10:02			0



DBs: USPAT

☑ Plurals

☑ Highlight all hit terms initially

Default operator: OR

```
generat$3 near10 (trigger adj1 output) near10 (trigger adj1
condition)
```

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
1	☐	☐	US 6618775 B1	20030909	28	DSP bus monitoring apparatus and method	710/100	712/35; 714/30;	
2	☐	☐	US 5226153 A	19930706	14	Bus monitor with time stamp means for independently	714/45	340/2.7; 702/187;	
3	☐	☐	US 5210862 A	19930511	16	Bus monitor with selective capture of independently	714/45		
4	☐	☐	US 5206948 A	19930427	14	Bus monitor with means for selectively capturing	714/45		
5	☐	☐	US 5142673 A	19920825	14	Bus monitor with dual port memory for storing	714/39		

Welcome to IEEE Xplore®

- ○ Home
- ○ What Can I Access?
- ○ Log-out

Tables of Contents

- ○ Journals & Magazines
- ○ Conference Proceedings
- ○ Standards

Search

- ○ By Author
- ○ Basic
- ○ Advanced

Member Services

- ○ Join IEEE
- ○ Establish IEEE Web Account
- ○ Access the IEEE Member Digital Library

IEEE Enterprise

- ○ Access the IEEE Enterprise File Cabinet

Print Format

Your search matched **8** of **1074479** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevanc** **Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enter new one in the text box.

generat* and trigger and condition and compar* Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

---

1 **Streamer current in a three-electrode system**
Akyuz, M.; Gao, L.; Cooray, V.; Larsson, A.;
Dielectrics and Electrical Insulation, IEEE Transactions on [see also Electrical Insulation, IEEE Transactions on] , Volume: 8 , Issue: 4 , Aug. 2001
Pages:665 - 672

[Abstract] [PDF Full-Text (728 KB)] **IEEE JNL**

---

2 **Charge carrier avalanche multiplication in high-voltage diodes trigg by ionizing radiation**
Soelkner, G.; Voss, P.; Kaindl, W.; Wachutka, G.; Maier, K.H.; Becker, H.-W.
Nuclear Science, IEEE Transactions on , Volume: 47 , Issue: 6 , Dec. 2000
Pages:2365 - 2372

[Abstract] [PDF Full-Text (201 KB)] **IEEE JNL**

---

3 **The breakdown fields and risetimes of select gases under the condi of fast charging (/spl sim/ 20 ns and less) and high pressures (20-1 atmospheres)**
Carboni, V.; Lackner, H.; Giri, D.; Lehr, J.;
Pulsed Power Plasma Science, 2001. PPPS-2001. Digest of Technical Papers , Volume: 1 , 17-22 June 2001
Pages:482 - 486 vol.1

[Abstract] [PDF Full-Text (487 KB)] **IEEE CNF**

---

4 **The influence of electron density on the formation of streamers in electrical discharges triggered with ultrashort laser pulses**
La Fontaine, B.; Vidal, F.; Comtois, D.; Ching-Yuan Chien; Desparois, A.; Joh T.W.; Kieffer, J.-C.; Mercure, H.P.; Pepin, H.; Rizk, F.A.M.;

Plasma Science, IEEE Transactions on , Volume: 27 , Issue: 3 , June 1999
Pages:688 - 700

[Abstract] [PDF Full-Text (248 KB)] **IEEE JNL**

---

5 **Analysis of a passive superconducting fault current limiter**
Cha, Y.S.; Zhongjin Yang; Turner, L.R.; Poeppel, R.B.;
Applied Superconductivity, IEEE Transactions on , Volume: 8 , Issue: 1 , Marc
1998
Pages:20 - 25

[Abstract] [PDF Full-Text (188 KB)] **IEEE JNL**

---

6 **Voltage pulse forming dynamics in a transmission line section empl
photoconductive charging and discharging**
Buck, J.A.; Kesler, M.P.;
Microwave Theory and Techniques, IEEE Transactions on , Volume: 42 , Issue
9 , Sept. 1994
Pages:1632 - 1637

[Abstract] [PDF Full-Text (504 KB)] **IEEE JNL**

---

7 **Dynamics of fibrin clot lysis under flow conditions by erythrocyte-li
tPA**
*Goel, M.S.; Murciano, J.-C.; Medinilla, S.; Yamamoto, A.; Cines, D.B.; Muzyk
V.R.; Diamond, S.L.;*
[Engineering in Medicine and Biology, 2002. 24th Annual Conference and the
Annual Fall Meeting of the Biomedical Engineering Society] EMBS/BMES
Conference, 2002. Proceedings of the Second Joint , Volume: 1 , 2002
Pages:520 vol.1

[Abstract] [PDF Full-Text (163 KB)] **IEEE CNF**

---

8 **The Atlas load protection switch**
*Davis, H.A.; Ballard, E.O.; Dorr, G.; Martinez, M.; Gribble, R.F.; Nielsen, K.E.
Pierce, D.; Parsons, W.M.;*
Pulsed Power Conference, 1999. Digest of Technical Papers. 12th IEEE
International , Volume: 2 , 27-30 June 1999
Pages:941 - 944 vol.2

[Abstract] [PDF Full-Text (420 KB)] **IEEE CNF**

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search | Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting | No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ| Terms | Back to Top

IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE

IEEE

Membership Publications/Services Standards Conferences Careers/Jobs

IEEE Xplore® RELEASE 1.8

Welcome
United States Patent and Trademark Office

Help FAQ Terms IEEE Peer Review

Quick Links

Welcome to IEEE Xplore®

- ○ Home
- ○ What Can I Access?
- ○ Log-out

Tables of Contents

- ○ Journals & Magazines
- ○ Conference Proceedings
- ○ Standards

Search

- ○ By Author
- ○ Basic
- ● Advanced

Member Services

- ○ Join IEEE
- ○ Establish IEEE Web Account
- ○ Access the IEEE Member Digital Library

IEEE Enterprise

- ○ Access the IEEE Enterprise File Cabinet

Search Results [PDF FULL-TEXT 420 KB] PREV DOWNLOAD CITATION

Request Permissions RIGHTSLINK

The Atlas load protection switch

Davis, H.A. Ballard, E.O. Dorr, G. Martinez, M. Gribble, R.F. Nielsen, K.E. Pierce, D. Parsons, W.M.
Los Alamos Nat. Lab., NM, USA;

This paper appears in: **Pulsed Power Conference, 1999. Digest of Technical Papers. 12th IEEE International**

Meeting Date: 06/27/1999 - 06/30/1999
Publication Date: 27-30 June 1999
Location: Monterey, CA USA
On page(s): 941 - 944 vol.2
Volume: 2
Reference Cited: 6
Number of Pages: 2 vol. 1529
Inspec Accession Number: 6537420

Abstract:

Atlas is a high-energy pulsed-power facility under development to study materials properties and hydrodynamics experiments under extreme **conditions**. Atlas will implode heavy liner loads (m~45 gm) with a peak current of 27-32 MA delivered in 4 μs, and is energized by 96, 240 kV Marx **generators** storing a total of 23 MJ. A key design requirement for Atlas is obtaining useful data for 95% of all loads installed on the

Print Format

machine. Materials response calculations show current from a prefire can damage the load requiring expensive and time consuming replacement. Therefore, we have incorporated a set of fast-acting mechanical switches in the Atlas design to reduce the probability of a prefire damaging the load. These switches, referred to as the load protection switches, short the load through a very low inductance path during system charge. Once the capacitors have reached full charge, the switches open on a time scale short **compared** to the bank charge time, allowing current to flow to the load when the **trigger** pulse is applied. The time window of vulnerability for load damage is thus substantially reduced. The design of the load protection switches and test results are presented

---

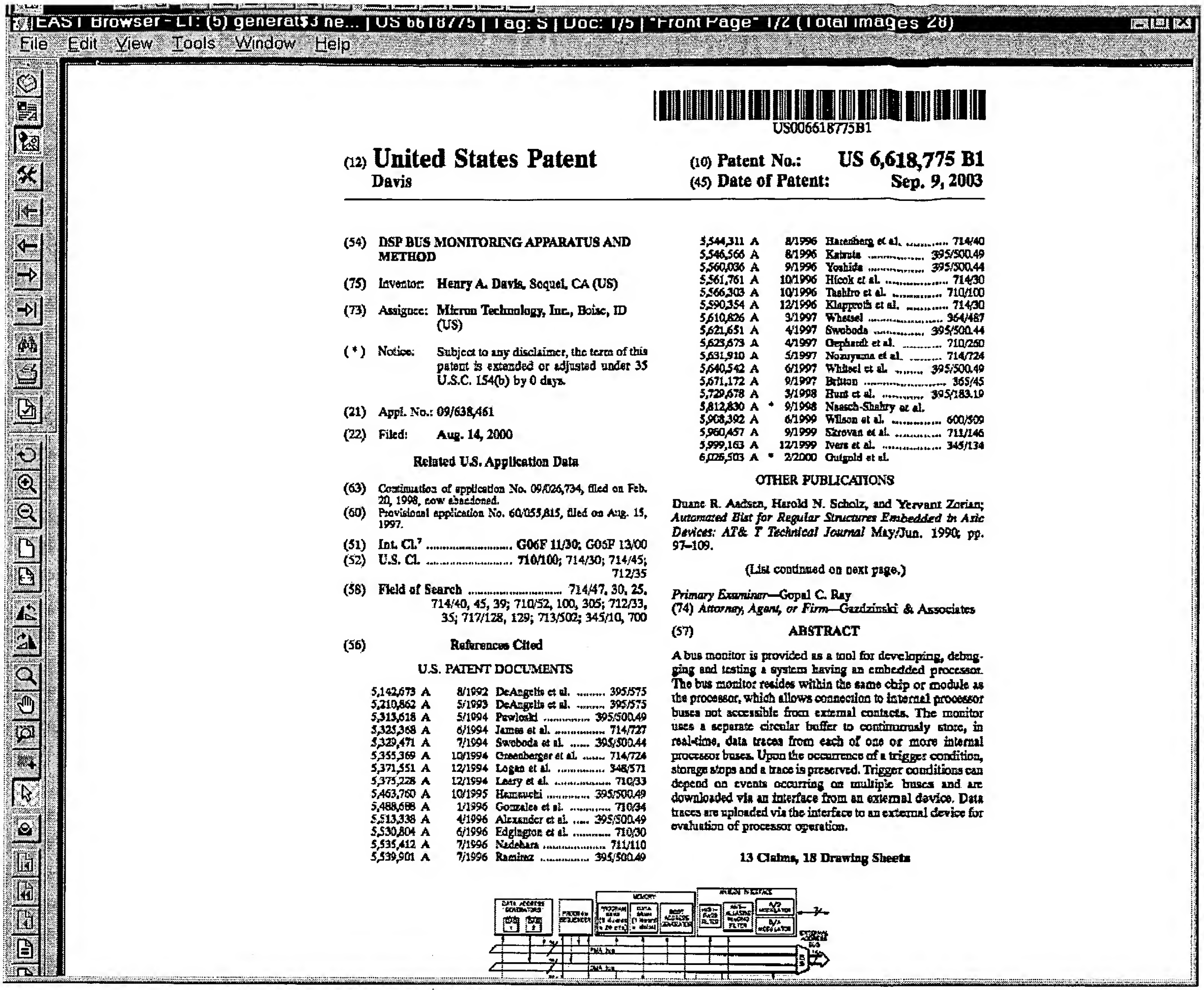
Index Terms:
protection pulse **generators** pulsed power supplies pulsed power switches 23 MJ 240 kV 27 to 32 MA 4 mus 45 g Atlas load protection switch Marx **generators** fast-acting mechanical switches heavy liner loads implosion high-energy pulsed-power facility hydrodynamics experiments materials properties materials response calculations prefire current **trigger** pulse very low inductance path

---

Documents that cite this document
There are no citing documents available in IEEE Xplore at this time.

Search Results [PDF FULL-TEXT 420 KB] PREV DOWNLOAD CITATION

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search | Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting | No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ| Terms | Back to Top



US006618775B1

(12) **United States Patent**
Davis

(10) **Patent No.: US 6,618,775 B1**
(45) **Date of Patent: Sep. 9, 2003**

(54) DSP BUS MONITORING APPARATUS AND METHOD

(75) Inventor: Henry A. Davis, Soquel, CA (US)

(73) Assignee: Micron Technology, Inc., Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/638,461

(22) Filed: Aug. 14, 2000

Related U.S. Application Data

(63) Continuation of application No. 09/026,734, filed on Feb. 20, 1998, now abandoned.
(60) Provisional application No. 60/055,815, filed on Aug. 15, 1997.

(51) Int. Cl.⁷ G06F 11/30; G05F 13/00
(52) U.S. Cl. 710/100; 714/30; 714/45; 712/35
(58) Field of Search 714/47, 30, 25, 714/40, 45, 39; 710/52, 100, 305; 712/33, 35; 717/128, 129; 713/502; 345/10, 700

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,142,673 A		8/1992	DeAngelis et al.	395/575
5,210,862 A		5/1993	DeAngelis et al.	395/575
5,313,618 A		5/1994	Pawloski	395/500.49
5,325,368 A		6/1994	James et al.	714/727
5,329,471 A		7/1994	Swoboda et al.	395/500.44
5,355,369 A		10/1994	Greenberger et al.	714/724
5,371,551 A		12/1994	Logan et al.	348/571
5,375,228 A		12/1994	Leary et al.	710/33
5,463,760 A		10/1995	Hamauchi	395/500.49
5,488,688 A		1/1996	Gonzales et al.	710/34
5,513,338 A		4/1996	Alexander et al.	395/500.49
5,530,804 A		6/1996	Edgington et al.	710/30
5,535,412 A		7/1996	Nadehara	711/110
5,539,901 A		7/1996	Ramirez	395/500.49
5,544,311 A		8/1996	Hatenberg et al.	714/40
5,546,566 A		8/1996	Katsuta	395/500.49
5,560,036 A		9/1996	Yoshida	395/500.44
5,561,761 A		10/1996	Hicok et al.	714/30
5,566,303 A		10/1996	Tashiro et al.	710/100
5,590,354 A		12/1996	Klapproth et al.	714/30
5,610,826 A		3/1997	Whetsel	364/487
5,621,651 A		4/1997	Swoboda	395/500.44
5,625,673 A		4/1997	Gephardt et al.	710/260
5,631,910 A		5/1997	Nozuyama et al.	714/724
5,640,542 A		6/1997	Whetsel et al.	395/500.49
5,671,172 A		9/1997	Britton	365/45
5,729,678 A		3/1998	Hunt et al.	395/183.19
5,812,830 A	*	9/1998	Naasch-Shahry et al.	
5,908,392 A		6/1999	Wilson et al.	600/509
5,960,457 A		9/1999	Skrovan et al.	711/146
5,999,163 A		12/1999	Ivers et al.	345/134
6,026,503 A	*	2/2000	Gutgold et al.	

OTHER PUBLICATIONS

Duane R. Aadsen, Harold N. Scholz, and Yervant Zorian; *Automated Bist for Regular Structures Embedded in Asic Devices: AT& T Technical Journal* May/Jun. 1990; pp. 97–109.

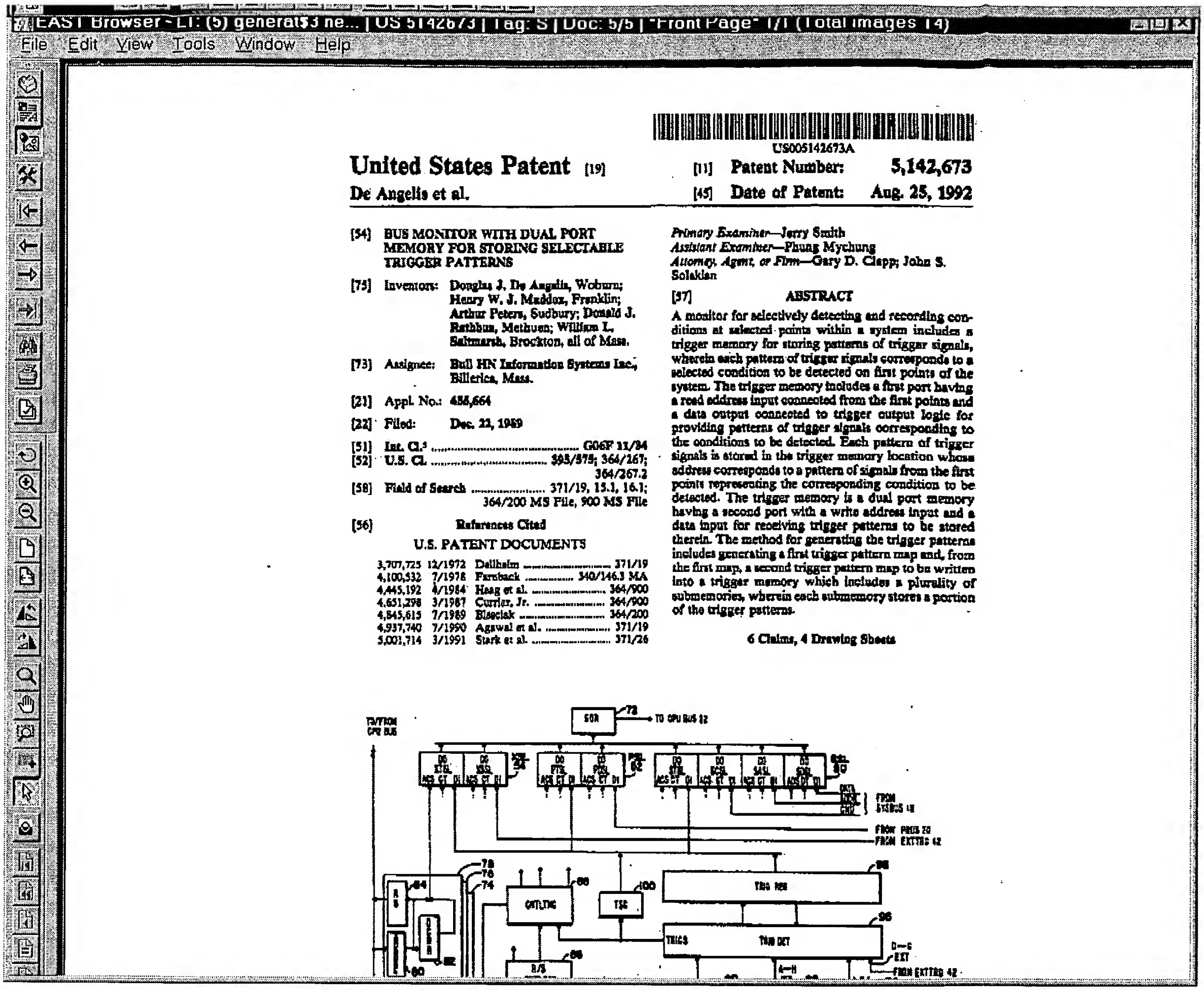
(List continued on next page.)

Primary Examiner—Gopal C. Ray
(74) *Attorney, Agent, or Firm*—Gazdzinski & Associates

(57) **ABSTRACT**

A bus monitor is provided as a tool for developing, debugging and testing a system having an embedded processor. The bus monitor resides within the same chip or module as the processor, which allows connection to internal processor buses not accessible from external contacts. The monitor uses a separate circular buffer to continuously store, in real-time, data traces from each of one or more internal processor buses. Upon the occurrence of a trigger condition, storage stops and a trace is preserved. Trigger conditions can depend on events occurring on multiple buses and are downloaded via an interface from an external device. Data traces are uploaded via the interface to an external device for evaluation of processor operation.

13 Claims, 18 Drawing Sheets



US005142673A

United States Patent [19]

De Angelis et al.

[11] **Patent Number: 5,142,673**

[45] **Date of Patent: Aug. 25, 1992**

[54] **BUS MONITOR WITH DUAL PORT MEMORY FOR STORING SELECTABLE TRIGGER PATTERNS**

[75] Inventors: Douglas J. De Angelis, Woburn; Henry W. J. Maddox, Franklin; Arthur Peters, Sudbury; Donald J. Rathbun, Methuen; William L. Saltmarsh, Brockton, all of Mass.

[73] Assignee: Bull HN Information Systems Inc., Billerica, Mass.

[21] Appl. No.: 456,664

[22] Filed: Dec. 22, 1989

[51] Int. Cl.^{5} G06F 11/34

[52] U.S. Cl. 395/575; 364/267; 364/267.2

[58] Field of Search .... 371/19, 15.1, 16.1; 364/200 MS File, 900 MS File

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,707,725	12/1972	Dellheim	371/19
4,100,532	7/1978	Farnbach	340/146.3 MA
4,445,192	4/1984	Haag et al.	364/900
4,651,298	3/1987	Currlin, Jr.	364/900
4,845,615	7/1989	Blasciak	364/200
4,937,740	7/1990	Agrawal et al.	371/19
5,001,714	3/1991	Stark et al.	371/26

Primary Examiner—Jerry Smith
Assistant Examiner—Phung Mychung
Attorney, Agent, or Firm—Gary D. Clapp; John S. Solakian

[57] **ABSTRACT**

A monitor for selectively detecting and recording conditions at selected points within a system includes a trigger memory for storing patterns of trigger signals, wherein each pattern of trigger signals corresponds to a selected condition to be detected on first points of the system. The trigger memory includes a first port having a read address input connected from the first points and a data output connected to trigger output logic for providing patterns of trigger signals corresponding to the conditions to be detected. Each pattern of trigger signals is stored in the trigger memory location whose address corresponds to a pattern of signals from the first points representing the corresponding condition to be detected. The trigger memory is a dual port memory having a second port with a write address input and a data input for receiving trigger patterns to be stored therein. The method for generating the trigger patterns includes generating a first trigger pattern map and, from the first map, a second trigger pattern map to be written into a trigger memory which includes a plurality of submemories, wherein each submemory stores a portion of the trigger patterns.

6 Claims, 4 Drawing Sheets

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs
Generate OACS

Search Results - Record(s) 1 through 9 of 9 returned.

☐ 1. Document ID: US 20030120980 A1

Using default format because multiple data bases are involved.

L8: Entry 1 of 9 File: PGPB Jun 26, 2003

PGPUB-DOCUMENT-NUMBER: 20030120980
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030120980 A1

TITLE: System trace unit

PUBLICATION-DATE: June 26, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Harris, Jeremy G.	Buckinghamshire		GB	

US-CL-CURRENT: 714/45

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. De

---

☐ 2. Document ID: US 6618775 B1

L8: Entry 2 of 9 File: USPT Sep 9, 2003

US-PAT-NO: 6618775
DOCUMENT-IDENTIFIER: US 6618775 B1
**** See image for Certificate of Correction ****

TITLE: DSP bus monitoring apparatus and method

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. De

---

☐ 3. Document ID: US 6378092 B1

L8: Entry 3 of 9 File: USPT Apr 23, 2002

US-PAT-NO: 6378092
DOCUMENT-IDENTIFIER: US 6378092 B1

TITLE: Integrated circuit testing

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

---

☐ 4. Document ID: US 5964893 A

L8: Entry 4 of 9 File: USPT Oct 12, 1999

US-PAT-NO: 5964893
DOCUMENT-IDENTIFIER: US 5964893 A

TITLE: Data processing system for performing a trace function and method therefor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

---

☐ 5. Document ID: US 5581745 A

L8: Entry 5 of 9 File: USPT Dec 3, 1996

US-PAT-NO: 5581745
DOCUMENT-IDENTIFIER: US 5581745 A

TITLE: Apparatus for suspending the bus cycle of a microprocessor by inserting wait states

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

---

☐ 6. Document ID: US 5226153 A

L8: Entry 6 of 9 File: USPT Jul 6, 1993

US-PAT-NO: 5226153
DOCUMENT-IDENTIFIER: US 5226153 A

TITLE: Bus monitor with time stamp means for independently capturing and correlating events

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

---

☐ 7. Document ID: US 5210862 A

L8: Entry 7 of 9 File: USPT May 11, 1993

US-PAT-NO: 5210862
DOCUMENT-IDENTIFIER: US 5210862 A

TITLE: Bus monitor with selective capture of independently occuring events from multiple sources

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

---

☐ 8. Document ID: US 5206948 A

L8: Entry 8 of 9 File: USPT Apr 27, 1993

US-PAT-NO: 5206948
DOCUMENT-IDENTIFIER: US 5206948 A

TITLE: Bus monitor with means for selectively capturing trigger conditions

Full | Title | Citation | Front | Review | Classification | Date | Reference | [illegible] | [illegible] | Claims | KWIC | Draw De

---

☐ 9. Document ID: US 5142673 A

L8: Entry 9 of 9 File: USPT Aug 25, 1992

US-PAT-NO: 5142673
DOCUMENT-IDENTIFIER: US 5142673 A

TITLE: Bus monitor with dual port memory for storing selectable trigger patterns

Full | Title | Citation | Front | Review | Classification | Date | Reference | [illegible] | [illegible] | Claims | KWIC | Draw De

---

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Terms	Documents
L5 and L7	9

Display Format: - Change Format

Previous Page Next Page Go to Doc#

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

☐ Generate Collection Print

L8: Entry 2 of 9 File: USPT Sep 9, 2003

US-PAT-NO: 6618775
DOCUMENT-IDENTIFIER: US 6618775 B1
**** See image for Certificate of Correction ****

TITLE: DSP bus monitoring apparatus and method

DATE-ISSUED: September 9, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Davis; Henry A.	Soquel	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Micron Technology, Inc.	Boise	ID			02

APPL-NO: 09/ 638461 [PALM]
DATE FILED: August 14, 2000

PARENT-CASE:
CROSS-REFERENCE TO RELATED APPLICATION This application is a continuation of U.S. patent application Ser. No. 09/026,734 filed Feb. 20, 1998 entitled "DSP Bus Monitoring Apparatus And Method", abandoned. Pursuant to 35 U.S.C. .sctn.119(e), this application claims the priority benefit of provisional application No. 60/055,815 filed Aug. 15, 1997.

INT-CL: [07] G06 F 11/30, G06 F 13/00

US-CL-ISSUED: 710/100; 714/30, 714/45, 712/35
US-CL-CURRENT: 710/100; 712/35, 714/30, 714/45

FIELD-OF-SEARCH: 714/47, 714/30, 714/25, 714/40, 714/45, 714/39, 710/52, 710/100, 710/305, 712/33, 712/35, 717/128, 717/129, 713/502, 345/10, 345/700

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5142673	August 1992	DeAngelis et al.	395/575
☐	5210862	May 1993	DeAngelis et al.	395/575
☐	5313618	May 1994	Pawloski	395/500.49

☐	5325368	June 1994	James et al.	714/727
☐	5329471	July 1994	Swoboda et al.	395/500.44
☐	5355369	October 1994	Greenberger et al.	714/724
☐	5371551	December 1994	Logan et al.	348/571
☐	5375228	December 1994	Leary et al.	710/33
☐	5463760	October 1995	Hamauchi	395/500.49
☐	5488688	January 1996	Gonzales et al.	710/34
☐	5513338	April 1996	Alexander et al.	395/500.49
☐	5530804	June 1996	Edgington et al.	710/30
☐	5535412	July 1996	Nadehara	711/110
☐	5539901	July 1996	Ramirez	395/500.49
☐	5544311	August 1996	Harenberg et al.	714/40
☐	5546566	August 1996	Katsuta	395/500.49
☐	5560036	September 1996	Yoshida	395/500.44
☐	5561761	October 1996	Hicok et al.	714/30
☐	5566303	October 1996	Tashiro et al.	710/100
☐	5590354	December 1996	Klapproth et al.	714/30
☐	5610826	March 1997	Whetsel	364/487
☐	5621651	April 1997	Swoboda	395/500.44
☐	5623673	April 1997	Gephardt et al.	710/260
☐	5631910	May 1997	Nozuyama et al.	714/724
☐	5640542	June 1997	Whitsel et al.	395/500.49
☐	5671172	September 1997	Britton	365/45
☐	5729678	March 1998	Hunt et al.	395/183.19
☐	5812830	September 1998	Naasch-Shahry et al.	
☐	5908392	June 1999	Wilson et al.	600/509
☐	5960457	September 1999	Skrovan et al.	711/146
☐	5999163	December 1999	Ivers et al.	345/134
☐	6026503	February 2000	Gutgold et al.	

OTHER PUBLICATIONS

Duane R. Aadsen, Harold N. Scholz, and Yervant Zorian; Automated Bist for Regular Structures Embedded in Asic Devices: AT& T Technical Journal May/Jun. 1990; pp. 97-109.
D. Mukherjee, C. Njinda and M.A. Breuer, Synthesis of Optimal 1-Hot Coded On-Chip Controllers for BIST Hardware; IEEE International Conference on Computer-Aided Design; Nov. 1991; pp. 236-239.
IEEE Computer Society; IEEE Standard Test Access Port and Boundary-Scan Architecture; Oct. 1993.
Debaditya Mukherjee, Massoud Pedram, and Melvin Breuer, Merging Multiple FSM Controllers for DFT/BIST Hardware; IEEE/ACM International Conference on Computer-

Aided Design; Nov. 1993; pp. 720-725.
Vishvani D. Agrawal, Chih-Jen Lin, Paul W. Rutkowski, Shianling Wu, and Yervant Zorian; Built-in Self-Test for Digital Integrated Circuits; AT& T Technical Journal; Mar./Apr. 1994; pp. 30-39.
Sybille Hellebrand, Hans-Joachim Wunderlich; An Efficient Procedure for the Synthesis of Fast Self-Testable Controller Structures; IEEE/ACM International Conference on Computer-Aided Design; Nov. 1994; pp. 110-116.
Albrecht P. Stroele and Hans-Joachim Wunderlich; Test Register Insertion with Minimum Hardware Cost; IEEE/ACM International Conference on Computer-Aided Design; Nov. 1995; pp. 95-101.
Takeshi Ikenaga and Takeshi Ogura; A Distributed BIST Technique and Its Test Design Platform for VLSIs; IECE Trans. Electron; vol. E78-C, No. 11; Nov. 1995; pp. 1618-1623.
Miodrag Potkonjak, Sujit Dey, Kazutoshi Wakabayashi, Design-For-Debugging of Application Specific Designs; IEEE/ACM International Conference on Computer-Aided Design; Nov. 1995; pp. 295-301.
Dan Strassberg; BIST: Pie in the Sky No Longer; EDN; Sep. 1996; pp. 77-85.
Karim Arabi, Bozena Kaminska and Janusz Rzeszut; BIST for D/A and A/D Converters; IEEE Computer Society; Winter 1996; pp. 49-49.
The Right Tools Do the Best Jobs; EDN; Jun., 1997; pp. S.cndot.10--S.cndot.21.

ART-UNIT: 2181

PRIMARY-EXAMINER: Ray; Gopal C.

ATTY-AGENT-FIRM: Gazdzinski & Associates

ABSTRACT:

A bus monitor is provided as a tool for developing, debugging and testing a system having an embedded processor. The bus monitor resides within the same chip or module as the processor, which allows connection to internal processor buses not accessible from external contacts. The monitor uses a separate circular buffer to continuously store, in real-time, data traces from each of one or more internal processor buses. Upon the occurrence of a trigger condition, storage stops and a trace is preserved. Trigger conditions can depend on events occurring on multiple buses and are downloaded via an interface from an external device. Data traces are uploaded via the interface to an external device for evaluation of processor operation.

13 Claims, 45 Drawing figures

Previous Doc Next Doc Go to Doc#